To all our customers

Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
   The information described here may contain technical inaccuracies or typographical errors.
   Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
   Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

Hitachi SuperH™RISC Engine

SH-3, SH3-DSP
SDRAM Interface

Application Notes

Application Notes ADE-502-074

Rev. 1.0
04/09/02
Hitachi, Ltd.

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

Preface

The SuperH™ RISC engine microcomputer is new generation RISC microcomputer that provides high-performance operations using a RISC-type CPU. This microcomputer also incorporates peripheral functions required for system configuration and achieves low-power consumption that is essential for all microcomputer application devices.

This SH-3, SH3-DSP SDRAM Interface Application Notes can be used as a reference for user system hardware design.

This application notes provides examples of SH-3 and SH3-DSP microcomputer interface with external memory (SDRAM).

Note that althrough the operations of task examples provided in this application notes have been checked by Hitachi, Ltd., it is advised that user check the operation of these task exanples prior to using the tasks in the user system.

Note: SuperH™ is a registered trademark of Hitachi, Ltd.

Contents

Section 1 How to Use the Application Notes

1.1 Configuration of SDRAM Interface Examples

The SDRAM interface examples (section 2) in this application notes consists of the following subsections to describe the SDRAM interface method.

- SDRAM interface examples in this application notes:
  - — Bus state controller (BSC) settings

    This subsection describes the BSC settings when SDRAM is connected.
  - — Interface circuit diagram

    This subsection shows SDRAM interface circuit examples.

Note that this application notes describes the SDRAM interfaces based on the MCU and SDRAM types summarized below.

MCU	SDRAM
SH7709A/SH7729	HM5225165ATT-A6
	HM5212165DTD-B60
	HM5264165TT-B60
SH7709	HM5212165D-B60
	HM5264165TT-B60
SH7708R	HM5212165D-B60
	HM5264165-B60

Section 2 SDRAM Interface Examples

2.1 SH7709A/SH7729 to SDRAM Interface Examples

2.1.1 Synchronous DRAM Direct Connection (SH7709A/SH7729)

Synchronous DRAM can be selected via the $\overline{CS}$ signal, and can be connected to areas 2 and 3 of the physical address space in the SH7709A or SH7729 by using common control signals such as $\overline{RAS}$. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 010, area 2 and area 3 can be used as the normal memory area and synchronous DRAM area, respectively. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 011, both areas 2 and 3 can be used as the synchronous DRAM area.

This LSI supports burst read/single write mode with burst length 1 as a synchronous DRAM operating mode. The data bus width can be selected as either 16 bits or 32 bits. The burst enable bit (BE) of MCR is ignored. In cache-fill/write-back cycles, 16-byte burst transfer is always performed. In write-through area write cycles or non-cacheable area read/write cycles, only one access is performed.

To connect this LSI to synchronous DRAM directly, the $\overline{RAS3L}$, $\overline{RAS3U}$, $\overline{CASL}$, $\overline{CASU}$, RD/$\overline{WR}$, $\overline{CS2}$ or $\overline{CS3}$, DQMUU, DQMUL, DQMLU, DQMLL, and CKE signals are used as control signals. These interface control signals, except for $\overline{CS2}$ and $\overline{CS3}$, are common to each area. In addition, the interface control signals other than CKE are valid and latched only when $\overline{CS2}$ or $\overline{CS3}$ is asserted. Accordingly, synchronous DRAM can be connected in parallel to multiple areas. The CKE signal is negated (brought low) only when self-refreshing is performed and the CKE signal is normally asserted (brought high).

The $\overline{RAS3L}$, $\overline{RAS3U}$, $\overline{CASL}$, and $\overline{CASU}$ signal outputs are determined depending on whether the address is in the upper or lower 32 Mbytes of each area. If the address is in the upper 32-Mbyte area (area 2: H'0A000000 to H'0BFFFFFF, area 3: H'0E000000 to H'0FFFFFFF), $\overline{RAS3U}$ and $\overline{CASU}$ are output. If it is in the lower 32-Mbyte area (area 2: H'08000000 to H'09FFFFFF, area 3: H'0C000000 to H'0DFFFFFF), $\overline{RAS3L}$ and $\overline{CASL}$ are output. In refresh cycles and mode-register write cycles, $\overline{RAS3U}$ and $\overline{RAS3L}$ or $\overline{CASU}$ and $\overline{CASL}$ are output.

The $\overline{RAS3L}$, $\overline{RAS3U}$, $\overline{CASL}$, $\overline{CASU}$ and RD/$\overline{WR}$ signals and specific address signals specify a command for synchronous DRAM. The synchronous DRAM commands are NOP, auto-refresh (REF), self-refresh (SELF), precharge all banks (PALL), row address strobe bank active (ACVT), read (READ), read with precharge (READA), write (WRIT), write with precharge (WRITA), and mode register setting (MRS).

Byte specification is performed by DQMUU, DQMUL, DQMLU, and DQMLL. A read/write is performed for the byte for which the corresponding DQM is low. In big-endian mode, DQMUU specifies an access to address 4n, and DQMLL specifies an access to address 4n + 3. In little-endian mode, DQMUU specifies an access to address 4n + 3, and DQMLL specifies an access to address 4n.

2.1.2 HM5225165ATT-A6 (4 Mwords × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5225165ATT-A6) are connected to area 3 of the SH7709A or SH7729 via a 16-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.1 lists the BSC register settings.

Note that the interface between SDRAM and the SH7709A or SH7729 is performed with bus clock = 66 MHz, CL = 2, TPC = 2, RCD = 2, TRWL = 1, and TRAS = 4.

Table 2.1 BSC Register Settings (HM5225165ATT-A6)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FF0	H'FFFFFF62	16	H'3FB0
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3FF3
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'522C
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A57C
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFFD000 to H'FFFFDFFF	8	Need not be set
	Area 3			H'FFFFE000 to H'FFFFEFFF		Write any value in address H'FFFFE440*
MCS0 control register		MCSCR0	H'0000	H'FFFFFF50	16	Need not be set
MCS1 control register		MCSCR1	H'0000	H'FFFFFF52	16	Need not be set
MCS2 control register		MCSCR2	H'0000	H'FFFFFF54	16	Need not be set
MCS3 control register		MCSCR3	H'0000	H'FFFFFF56	16	Need not be set
MCS4 control register		MCSCR4	H'0000	H'FFFFFF58	16	Need not be set
MCS5 control register		MCSCR5	H'0000	H'FFFFFF5A	16	Need not be set
MCS6 control register		MCSCR6	H'0000	H'FFFFFF5C	16	Need not be set
MCS7 control register		MCSCR7	H'0000	H'FFFFFF5E	16	Need not be set

Note: Bits not related to this interface example show initial values. All register settings must be checked according to the user system.

* In area 3, the SDMR address is determined by adding H'FFFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.1 shows an interface circuit for the case in which area 3 of the SH7709A or SH7729 is connected to SDRAM (HM5225165ATT-A6) via a 16-bit bus.

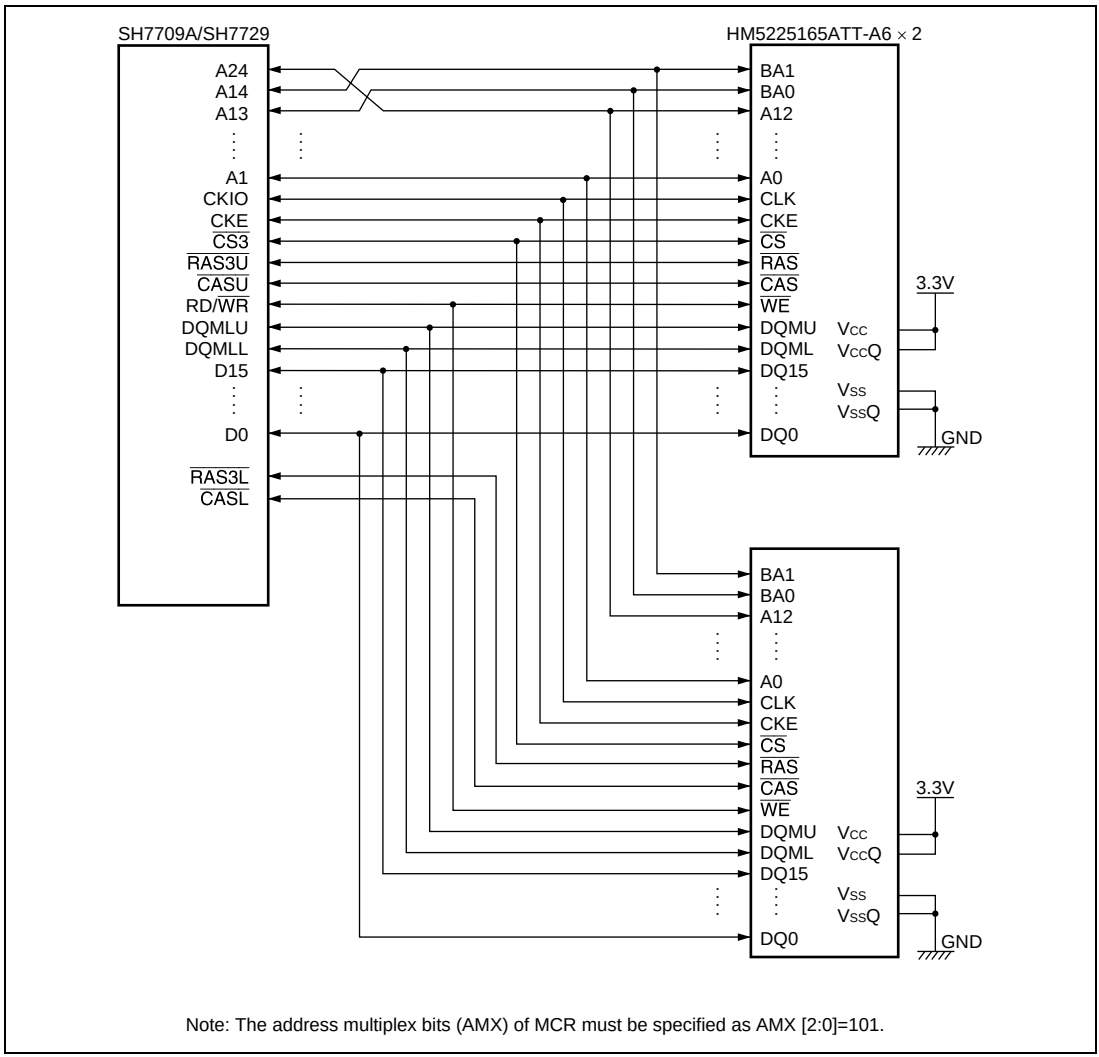


Figure 2.1 Interface between SDRAM (HM5225165ATT-A6) and SH7709A or SH7729

2.1.3 HM5212165DTD-B60 (2 Mwords × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5212165DTD-B60) are connected to area 3 of the SH7709A or SH7729 via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.2 lists the BSC register settings.

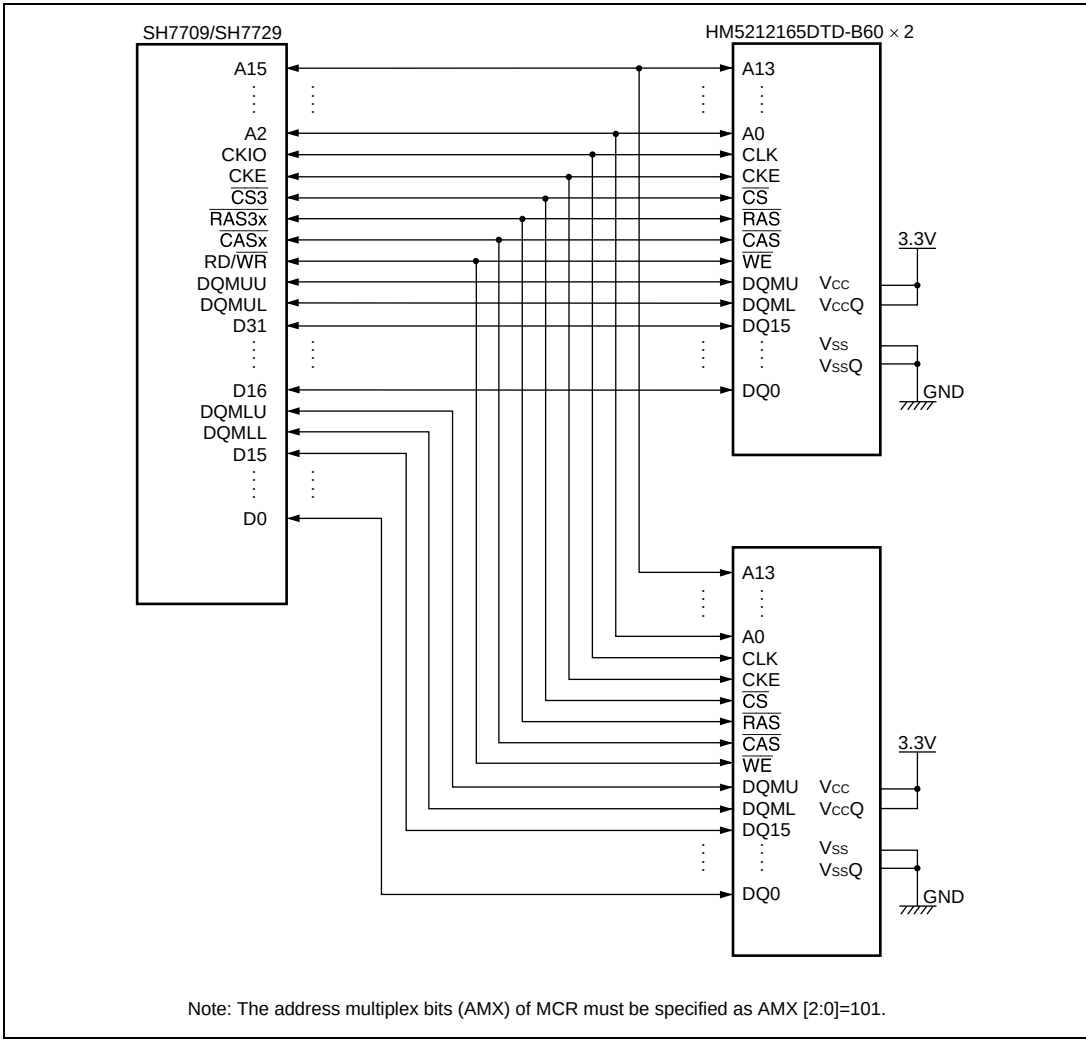
Note that the interface between SDRAM and the SH7709A or SH7729 is performed with bus clock = 66 MHz, CL = 2, TPC = 2, RCD = 2, TRWL = 1, and TRAS = 4.

Table 2.2 BSC Register Settings (HM5212165DTD-B60)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FF0	H'FFFFFF62	16	H'3FF0
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3FF3
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'522C
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A5F8
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFFD000 to H'FFFFDFFF	8	Need not be set
	Area 3			H'FFFFE000 to H'FFFFEFFF		Write any value in address H'FFFFE880*
MCS0 control register		MCSCR0	H'0000	H'FFFFFF50	16	Need not be set
MCS1 control register		MCSCR1	H'0000	H'FFFFFF52	16	Need not be set
MCS2 control register		MCSCR2	H'0000	H'FFFFFF54	16	Need not be set
MCS3 control register		MCSCR3	H'0000	H'FFFFFF56	16	Need not be set
MCS4 control register		MCSCR4	H'0000	H'FFFFFF58	16	Need not be set
MCS5 control register		MCSCR5	H'0000	H'FFFFFF5A	16	Need not be set
MCS6 control register		MCSCR6	H'0000	H'FFFFFF5C	16	Need not be set
MCS7 control register		MCSCR7	H'0000	H'FFFFFF5E	16	Need not be set

Note: * In area 3, the SDMR address is determined by adding H'FFFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.2 shows an interface circuit for the case in which area 3 of the SH7709A or SH7729 is connected to SDRAM (HM5212165DTD-B60) via a 32-bit bus.



Note: The address multiplex bits (AMX) of MCR must be specified as AMX [2:0]=101.

Figure 2.2 Interface between SDRAM (HM5212165DTD-B60) and SH7709A or SH7729

2.1.4 HM5264165TT-B60 (1 Mword × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5264165TT-B60) are connected to area 3 of the SH7709A or SH7729 via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.3 lists the BSC register settings.

Note that the interface between SDRAM and the SH7709A or SH7729 is performed with bus clock = 66 MHz, CL = 2, TPC = 2, RCD = 3, TRWL = 1, and TRAS = 4.

Table 2.3 BSC Register Settings (HM5264165TT-B60)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FF0	H'FFFFFF62	16	H'3FF0
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3FF3
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'6224
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A5F8
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFFD000 to H'FFFFDFFF	8	Need not be set
	Area 3			H'FFFFE000 to H'FFFFEFFF		Write any value in address H'FFFFE880*
MCS0 control register		MCSCR0	H'0000	H'FFFFFF50	16	Need not be set
MCS1 control register		MCSCR1	H'0000	H'FFFFFF52	16	Need not be set
MCS2 control register		MCSCR2	H'0000	H'FFFFFF54	16	Need not be set
MCS3 control register		MCSCR3	H'0000	H'FFFFFF56	16	Need not be set
MCS4 control register		MCSCR4	H'0000	H'FFFFFF58	16	Need not be set
MCS5 control register		MCSCR5	H'0000	H'FFFFFF5A	16	Need not be set
MCS6 control register		MCSCR6	H'0000	H'FFFFFF5C	16	Need not be set
MCS7 control register		MCSCR7	H'0000	H'FFFFFF5E	16	Need not be set

Note: * In area 3, the SDMR address is determined by adding H'FFFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.3 shows an interface circuit for the case in which area 3 of the SH7709A or SH7729 is connected to SDRAM (HM5264165TT-B60) via a 32-bit bus.

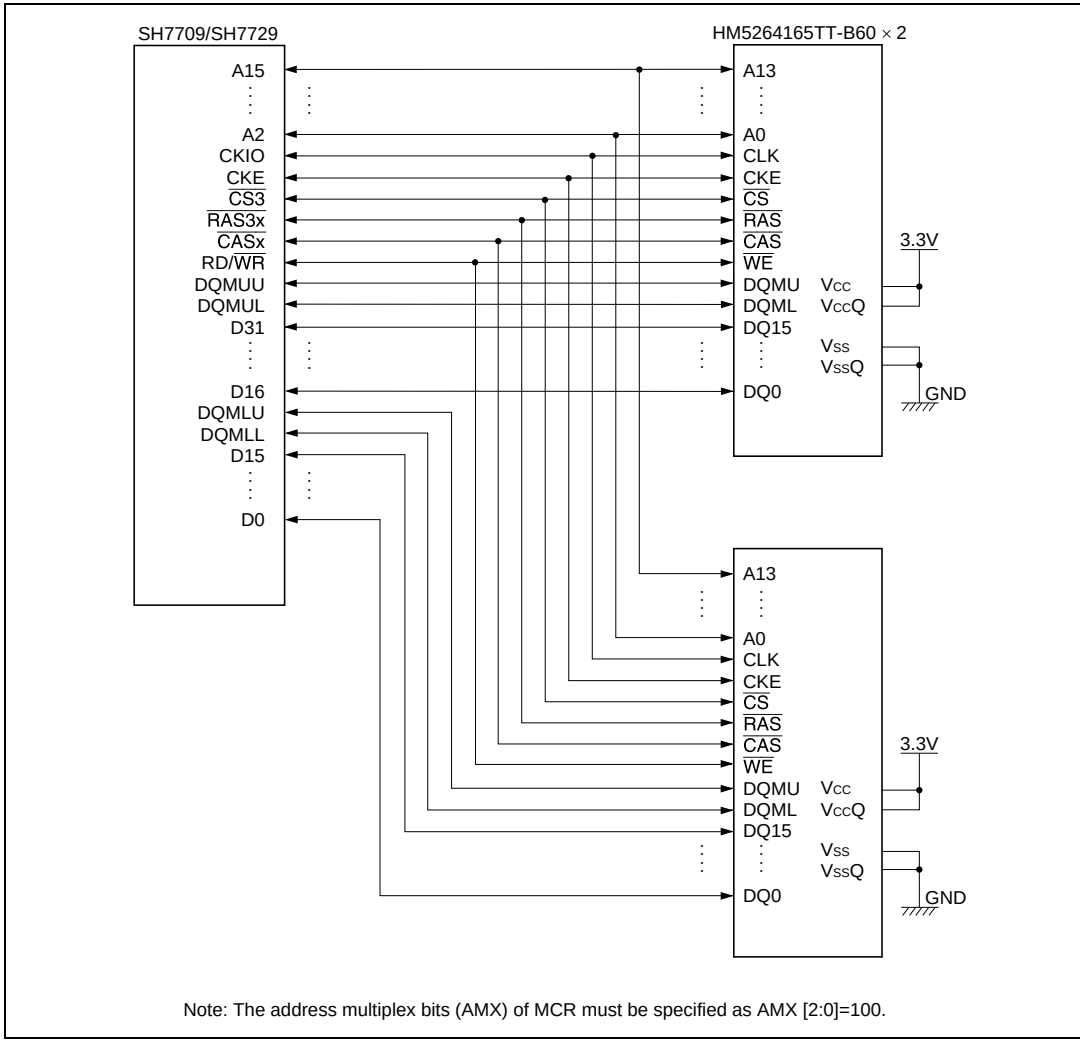


Figure 2.3 Interface between SDRAM (HM5264165TT-B60) and SH7709A or SH7729

2.1.5 Power-On Sequence (SH7709A/SH7729)

To use the synchronous DRAM, specify modes after power-on. To initialize the synchronous DRAM correctly, first specify the bus state controller registers and then specify the synchronous DRAM mode register. When specifying the synchronous DRAM mode register, the address signal value is latched depending on the combination of $\overline{RAS}$, $\overline{CAS}$, and RD/$\overline{WR}$ signals. In this case, the bus state controller functions as follows. To write a designated value X to the DRAM mode register, write data to address H'FFFFD000 + X for area 2 of synchronous DRAM and write data to H'FFFFE000 + X for area 3 of synchronous DRAM. At this time, data written at addresses H'FFFFD000 + X and H'FFFFE000 + X is ignored and the DRAM mode register is written in byte units.

To specify burst read/single write, CAS latency as 1 to 3, sequential as lap type, and burst length as 1, write arbitrary data in byte units to the addresses listed below.

		Area 2	**Area 3**
32-bit bus width	CAS latency 1	FFFD840	FFFE840
	CAS latency 2	FFFD880	FFFE880
	CAS latency 3	FFFD8C0	FFFE8C0
		Area 2	**Area 3**
16-bit bus width	CAS latency 1	FFFD420	FFFE420
	CAS latency 2	FFFD440	FFFE440
	CAS latency 3	FFFD460	FFFE460

By writing data to address H'FFFD000 + X or address H'FFFE000 + X, the precharge all banks command (PALL) is first issued at cycle TRp1, and a mode register write command is issued at the following cycle TMw1. The address signals when a mode register write command is issued are as follows.

32-bit bus width	A15 to A9	0000100 (Burst read and single write)
	A8 to A6	CAS latency
	A5	0 (Burst type = sequential)
	A4 to A2	000 (Burst length 1)
16-bit bus width	A14 to A8	0000100 (Burst read and single write)
	A7 to A5	CAS latency
	A4	0 (Burst type = sequential)
	A3 to A1	000 (Burst length 1)

Before specifying the mode register, 100 µs of idle time (differs depending on the memory manufacturer) required for synchronous DRAM must be ensured after power-on. If the pulse width of the reset signal is longer than this idle time, the mode register can be specified immediately after power-on. In addition, dummy auto-refresh cycles must be executed for the number of times specified by the manufacturer (normally 8 times) or more. Dummy auto-refresh cycles are normally specified to be executed automatically during initializations after auto-refresh setting. However, to ensure execution of the auto-refresh cycles, the time intervals between refresh requests must be shortened while the dummy cycles are executed. Note that the auto-refresh cycles must be executed in order to initialize the synchronous DRAM internal address counter because the synchronous DRAM internal address counter cannot be initialized by a normal read or write access.

2.2 SH7709 and SDRAM Interface Examples

2.2.1 Synchronous DRAM Direct Connection (SH7709)

Synchronous DRAM can be selected via the $\overline{CS}$ signal, and can be connected to areas 2 and 3 of the physical address space in the SH7709A or SH7729 by using common control signals such as RAS. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 010, area 2 and area 3 can be used as the normal memory area and synchronous DRAM area, respectively. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 011, both areas 2 and 3 can be used as the synchronous DRAM area.

This LSI supports burst read/single write mode with burst length 1 as a synchronous DRAM operating mode. The data bus width can be selected as either 16 bits or 32 bits. The burst enable bit (BE) of MCR is ignored. In cache-fill/write-back cycles, 16-byte burst transfer is always performed. In write-through area write cycles or non-cacheable area read/write cycles, only one access is performed.

To connect this LSI to synchronous DRAM directly, the $\overline{RAS3L}$, $\overline{RAS3U}$, $\overline{CASL}$, $\overline{CASU}$, RD/$\overline{WR}$, $\overline{CS2}$ or $\overline{CS3}$, DQMUU, DQMUL, DQMLU, DQMLL, and CKE signals are used as control signals. These interface control signals, except for $\overline{CS2}$ and $\overline{CS3}$, are common to each area. In addition, the interface control signals other than CKE are valid and latched only when $\overline{CS2}$ or $\overline{CS3}$ is asserted. Accordingly, synchronous DRAM can be connected in parallel to multiple areas. The CKE signal is negated (brought low) only when self-refreshing is performed and the CKE signal is normally asserted (brought high).

The $\overline{RAS3L}$, $\overline{RAS3U}$, $\overline{CASL}$, and $\overline{CASU}$ signal outputs are determined depending on whether the address is in the upper or lower 32 Mbytes of each area. If the address is in the upper 32-Mbyte area (area 2: H'0A000000 to H'0BFFFFFF, area 3: H'0E000000 to H'0FFFFFFF), $\overline{RAS3U}$ and $\overline{CASU}$ are output. If it is in the lower 32-Mbyte area (area 2: H'08000000 to H'09FFFFFF, area 3: H'0C000000 to H'0DFFFFFF), $\overline{RAS3L}$ and $\overline{CASL}$ are output. In refresh cycles and mode-register write cycles, $\overline{RAS3U}$ and $\overline{RAS3L}$ or $\overline{CASU}$ and $\overline{CASL}$ are output.

The $\overline{\text{RAS3L}}$, $\overline{\text{RAS3U}}$, $\overline{\text{CASL}}$, $\overline{\text{CASU}}$ and RD/$\overline{\text{WR}}$ signals and specific address signals specify a command for synchronous DRAM. The synchronous DRAM commands are NOP, auto-refresh (REF), self-refresh (SELF), precharge all banks (PALL), row address strobe bank active (ACVT), read (READ), read with precharge (READA), write (WRIT), write with precharge (WRITA), and mode register setting (MRS).

Byte specification is performed by DQMUU, DQMUL, DQMLU, and DQMLL. A read/write is performed for the byte for which the corresponding DQM is low. In big-endian mode, DQMUU specifies an access to address 4n, and DQMLL specifies an access to address 4n + 3. In little-endian mode, DQMUU specifies an access to address 4n + 3, and DQMLL specifies an access to address 4n.

2.2.2 HM5212165D-B60 (2 Mwords × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5212165D-B60) are connected to area 3 of the SH7709 via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.4 lists the BSC register settings.

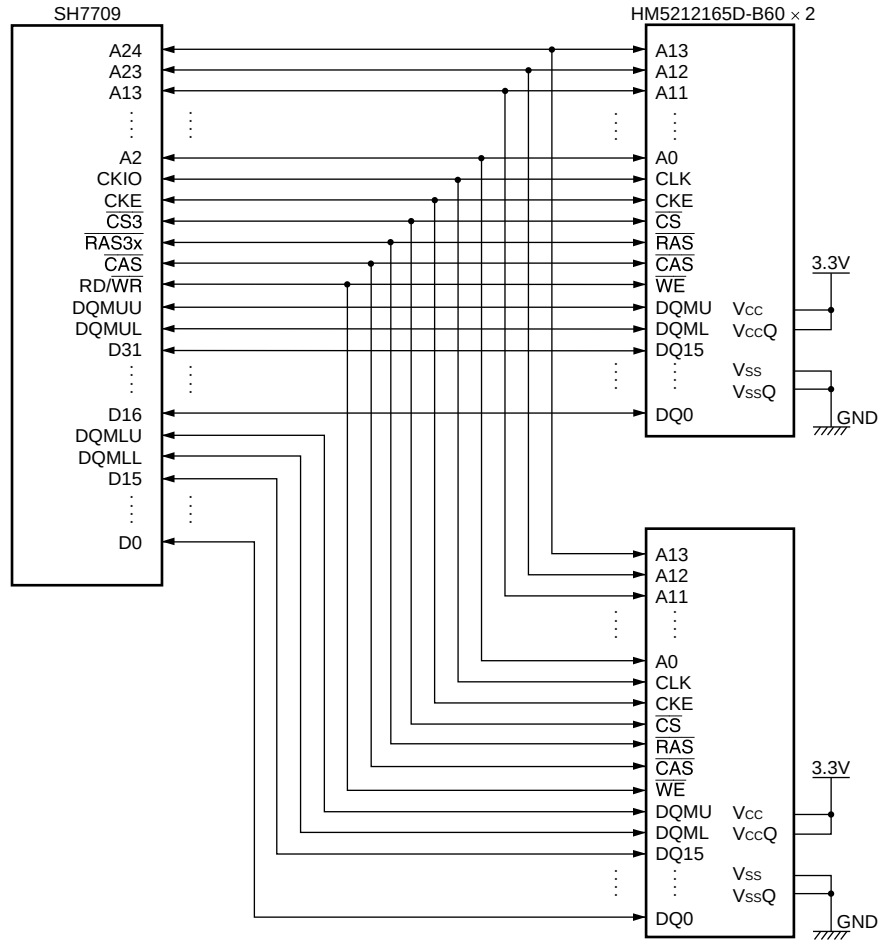
Note that the interface between SDRAM and the SH7709 is performed with bus clock = 40 MHz, CL = 2, TPC = 1, RCD = 1, TRWL = 1, and TRAS = 2.

Table 2.4 BSC Register Settings (HM5212165D-B60)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FF0	H'FFFFFF62	16	H'3FF0
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3F33
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'000C
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A54F
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFFD000 to H'FFFFDFFF	8	Need not be set
	Area 3			H'FFFFE000 to H'FFFFEFFF		Write any value in address H'FFFFE880*

Note: * In area 3, the SDMR address is determined by adding H'FFFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.4 shows an interface circuit for the case in which area 3 of the SH7709 is connected to SDRAM (HM5212165D-B60) via a 32-bit bus.



Note: Upper addresses of the SH7709, which are not multiplexed with other pin functions, are used for SDRAM bank selection. In this interface example, A23 and A24 of the SH7709 are used. The address multiplex bits (AMX) of MCR must be specified as AMX[1:0]=01. Note that only the upper or lower 32 Mbytes in a 64-Mbyte address space can be used.

Figure 2.4 Interface between SDRAM (HM5212165D-B60) and SH7709

2.2.3 HM5264165TT-B60 (1 Mword × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5264165TT-B60) are connected to area 3 of the SH7709 via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.5 lists the BSC register settings.

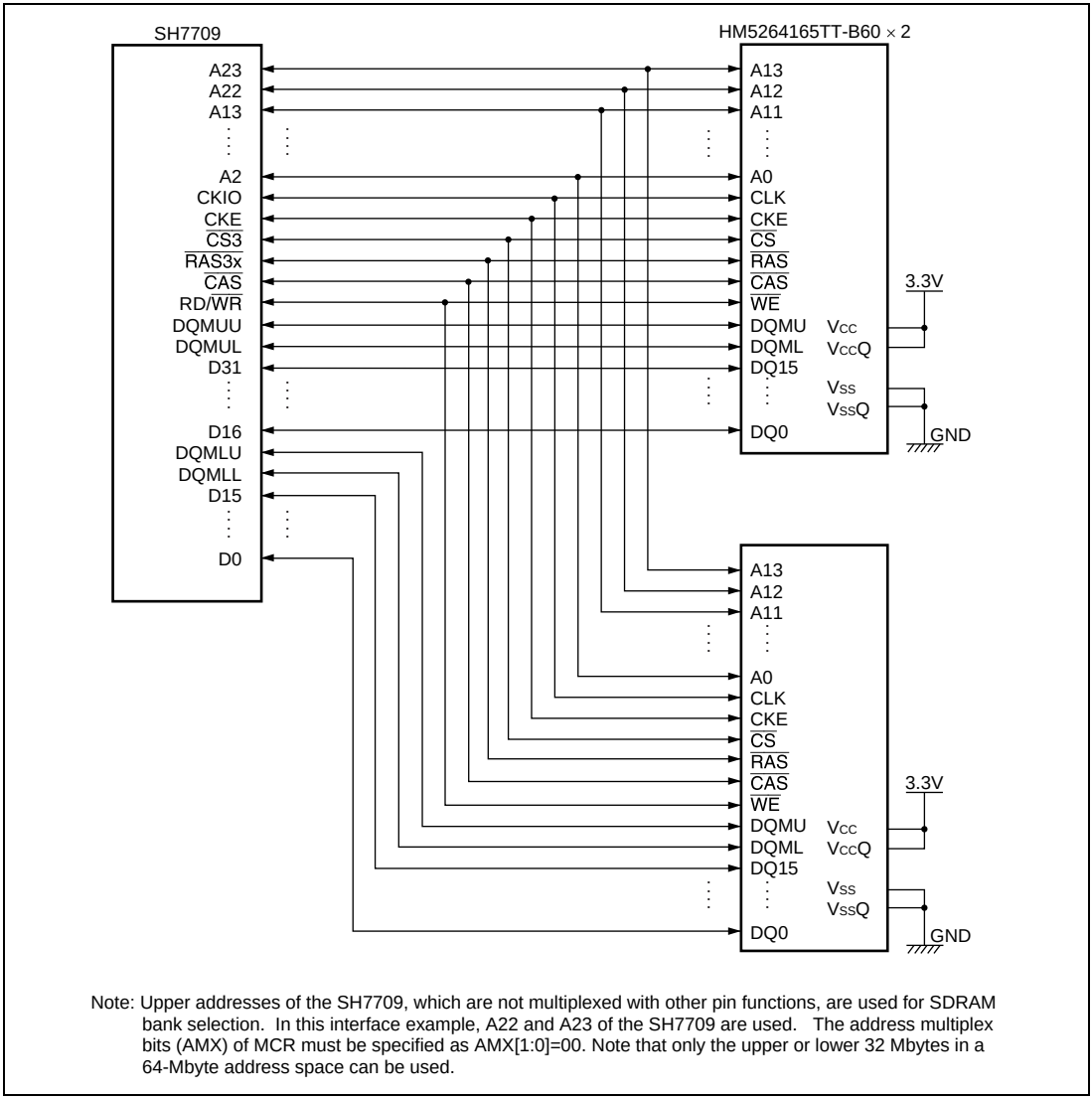
Note that the interface between SDRAM and the SH7709 is performed with bus clock = 40 MHz, CL = 2, TPC = 1, RCD = 1, TRWL = 1, and TRAS = 2.

Table 2.5 BSC Register Settings (HM5264165TT-B60)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FF0	H'FFFFFF62	16	H'3FF0
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3F33
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'0004
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A54F
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFFD000 to H'FFFFDFFF	8	Need not be set
	Area 3			H'FFFFE000 to H'FFFFEFFF		Write any value in address H'FFFFE880*

Note: * In area 3, the SDMR address is determined by adding H'FFFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.5 shows an interface circuit for the case in which area 3 of the SH7709 is connected to SDRAM (HM5264165TT-B60) via a 32-bit bus.



Note: Upper addresses of the SH7709, which are not multiplexed with other pin functions, are used for SDRAM bank selection. In this interface example, A22 and A23 of the SH7709 are used. The address multiplex bits (AMX) of MCR must be specified as AMX[1:0]=00. Note that only the upper or lower 32 Mbytes in a 64-Mbyte address space can be used.

Figure 2.5 Interface between SDRAM (HM5264165TT-B60) and SH7709

2.2.4 Power-On Sequence (SH7709)

To use the synchronous DRAM, specify modes after power-on. To initialize the synchronous DRAM correctly, first specify the bus state controller registers and then specify the synchronous DRAM mode register. When specifying the synchronous DRAM mode register, the address signal value is latched depending on the combination of $\overline{RAS}$, $\overline{CAS}$, and RD/$\overline{WR}$ signals. In this case, the bus state controller functions as follows. To write a designated value X to the DRAM mode register, write data to address H'FFFFD000 + X for area 2 of synchronous DRAM and write data to H'FFFFE000 + X for area 3 of synchronous DRAM. At this time, data written at addresses H'FFFFD000 + X and H'FFFFE000 + X is ignored and the DRAM mode register is written in byte units.

To specify burst read/single write, CAS latency as 1 to 3, sequential as lap type, and burst length as 1, write arbitrary data in byte units to the addresses listed below.

	Area 2	**Area 3**
CAS latency 1	FFFD840	FFFE840
CAS latency 2	FFFD880	FFFE880
CAS latency 3	FFFD8C0	FFFE8C0

By writing data to address H'FFFD000 + X or address H'FFFE000 + X, the precharge all banks command (PALL) is first issued at cycle TRp1, and a mode register write command is issued at the following cycle TMw1.

Before specifying the mode register, 100 µs of idle time (differs depending on the memory manufacturer) required for synchronous DRAM must be ensured after power-on. If the pulse width of the reset signal is longer than this idle time, the mode register can be specified immediately after power-on. In addition, dummy auto-refresh cycles must be executed for the number of times specified by the manufacturer (normally 8 times) or more. Dummy auto-refresh cycles are normally specified to be executed automatically during initializations after auto-refresh setting. However, to ensure execution of the auto-refresh cycles, the time intervals between refresh requests must be shortened while the dummy cycles are executed. Note that the auto-refresh cycles must be executed in order to initialize the synchronous DRAM internal address counter because the synchronous DRAM internal address counter cannot be initialized by a normal read or write access.

2.3 SH7708R and SDRAM Interface Examples

2.3.1 Synchronous DRAM Direct Connection (SH7708R)

Synchronous DRAM can be selected via the $\overline{CS}$ signal, and can be connected to area 2 and area 3 of the physical space in the SH7708R by using common control signals such as $\overline{RAS}$. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 010, area 2 and area 3 are used as the normal memory area and synchronous DRAM area, respectively. When the memory type bits (DRAMTP2 to DRAMTP0) of BCR1 are set to 011, both areas 2 and 3 are used as the synchronous DRAM area.

This LSI supports burst read/single write mode with burst length 1 as a synchronous DRAM operating mode. The data bus width is fixed at 32 bits, and the size bit (SZ) of MCR must always be set to 1. The burst enable bit (BE) of MCR is ignored. Accordingly, 16-byte burst transfer is always performed in cache-fill/write-back cycles, and only one access is performed in write-through area write cycles or non-cacheable area read/write cycles.

To connect this LSI to synchronous DRAM directly, the $\overline{RAS3L}$, $\overline{RAS3U}$, $\overline{CASL}$, $\overline{CASU}$, RD/$\overline{WR}$, $\overline{CS2}$ or $\overline{CS3}$, DQMUU, DQMUL, DQMLU, DQMLL, and CKE signals are used as control signals. These interface control signals, except for $\overline{CS2}$ and $\overline{CS3}$, are common to each area. In addition, the interface control signals other than CKE are valid and latched only when $\overline{CS2}$ or $\overline{CS3}$ is asserted. Accordingly, synchronous DRAM can be connected in parallel to multiple areas. The CKE signal is negated (brought low) only when self-refreshing is performed and the CKE signal is normally asserted (brought high).

The $\overline{RAS3L}$, $\overline{RAS3U}$, $\overline{CASL}$, $\overline{CASU}$ and RD/$\overline{WR}$ signals and specific address signals specify a command for synchronous DRAM. The synchronous DRAM commands are NOP, auto-refresh (REF), self-refresh (SELF), precharge all banks (PALL), row address strobe bank active (ACVT), read (READ), read with precharge (READA), write (WRIT), write with precharge (WRITA), and mode register setting (MRS).

Byte specification is performed by DQMUU, DQMUL, DQMLU, and DQMLL. A read/write is performed for the byte for which the corresponding DQM is low. In big-endian mode, DQMUU specifies an access to address 4n, and DQMLL specifies an access to address 4n + 3. In little-endian mode, DQMUU specifies an access to address 4n + 3, and DQMLL specifies an access to address 4n.

2.3.2 HM5212165D-B60 (2 Mwords × 16 bits × 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5212165D-B60) are connected to area 3 of the SH7708R via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.6 lists the BSC register settings.

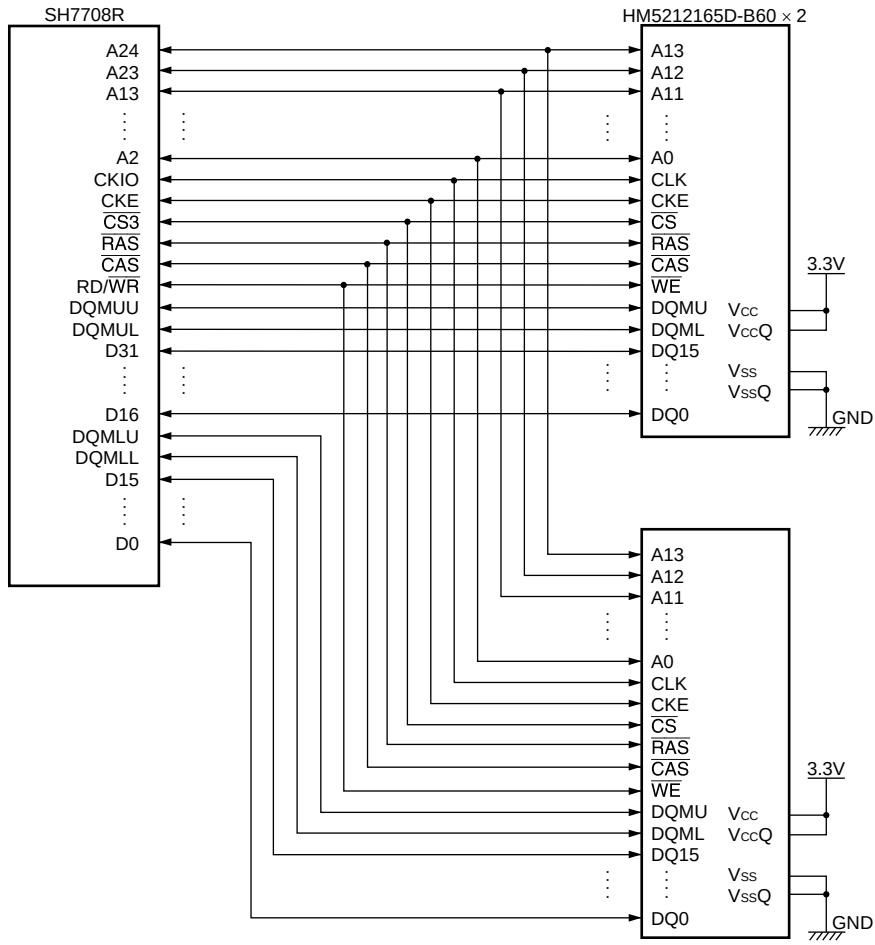
Note that the interface between SDRAM and the SH7708R is performed with bus clock = 60 MHz, CL = 2, TPC = 1, RCD = 1, TRWL = 1, and TRAS = 2.

Table 2.6 BSC Register Settings (HM5212165D-B60)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FFC	H'FFFFFF62	16	H'3FFC
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3FFF
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'000C
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A5EB
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	–	H'FFFFD000 to H'FFFFDFFF	8	Need not be set
	Area 3			H'FFFFE000 to H'FFFFEFFF		Write any value in address H'FFFFE880*

Note: * In area 3, the SDMR address is determined by adding H'FFFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.6 shows an interface circuit for the case in which area 3 of the SH7708R is connected to SDRAM (HM5212165D-B60) via a 32-bit bus.



Note: Upper addresses of the SH7708R, which are not multiplexed with other pin functions, are used for SDRAM bank selection. In this interface example, A23 and A24 of the SH7708R are used. The address multiplex bits (AMX) of MCR must be specified as AMX[1:0]=01.

Figure 2.6 Interface between SDRAM (HM5212165D-B60) and SH7708R

2.3.3 HM5264165-B60 (1 Mword x 16 bits x 4 banks)

Bus State Controller (BSC) Settings: When two SDRAMs (HM5264165-B60) are connected to area 3 of the SH7708R via a 32-bit bus, the bus state controller (BSC) must be specified as summarized below. Table 2.7 lists the BSC register settings.

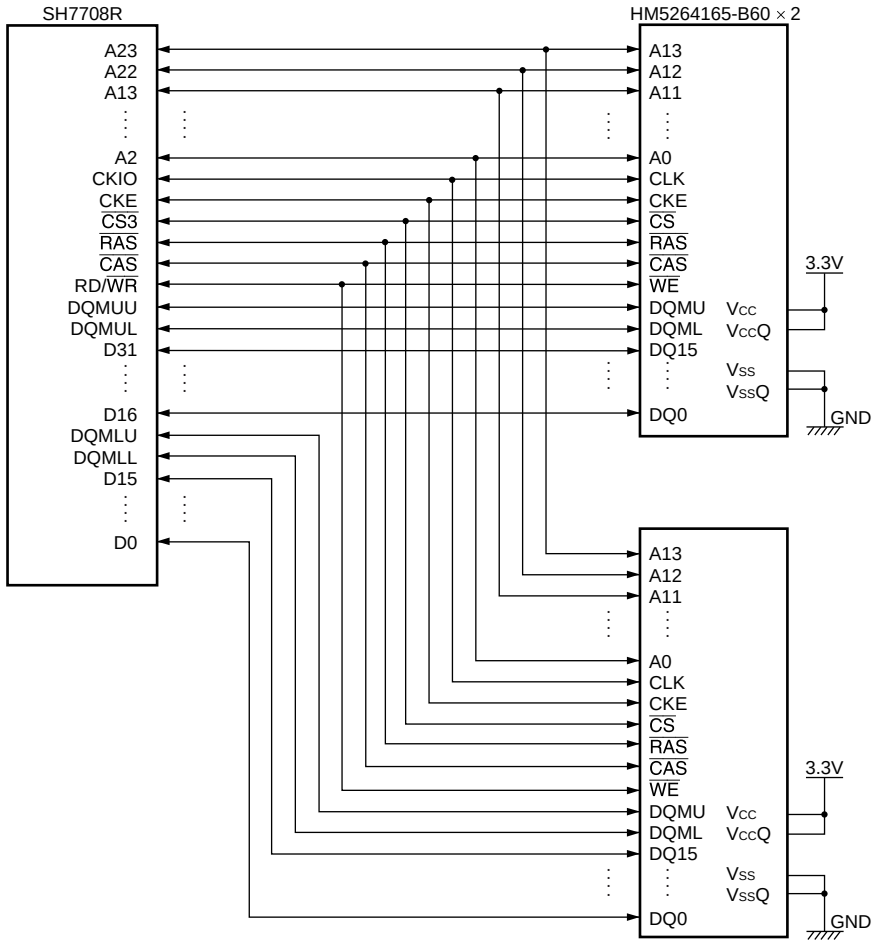
Note that the interface between SDRAM and the SH7708R is performed with bus clock = 60 MHz, CL = 2, TPC = 1, RCD = 1, TRWL = 1, and TRAS = 2.

Table 2.7 BSC Register Settings (HM5264165-B60)

Register Name		Abbr.	Initial Value	Address	Access Size	Setting Value
Bus control register 1		BCR1	H'0000	H'FFFFFF60	16	H'0008
Bus control register 2		BCR2	H'3FFC	H'FFFFFF62	16	H'3FFC
Wait state control register 1		WCR1	H'3FF3	H'FFFFFF64	16	H'3FFF
Wait state control register 2		WCR2	H'FFFF	H'FFFFFF66	16	H'FFDF
Individual memory control register		MCR	H'0000	H'FFFFFF68	16	H'0004
DRAM control register		DCR	H'0000	H'FFFFFF6A	16	Need not be set
PCMCIA control register		PCR	H'0000	H'FFFFFF6C	16	Need not be set
Refresh timer control/status register		RTCSR	H'0000	H'FFFFFF6E	16	H'A508
Refresh timer counter		RTCNT	H'0000	H'FFFFFF70	16	H'A500
Refresh time constant counter		RTCOR	H'0000	H'FFFFFF72	16	H'A582
Refresh count register		RFCR	H'0000	H'FFFFFF74	16	Need not be set
Bus control register 3		BCR3	H'0000	H'FFFFFF7E	16	Need not be set
Synchronous DRAM mode register	Area 2	SDMR	—	H'FFFFD000 to H'FFFFDFFF	8	Need not be set
	Area 3			H'FFFFE000 to H'FFFFEFFF		Write any value in address H'FFFFE880*

Note: * In area 3, the SDMR address is determined by adding H'FFFFE000 to the desired value to be set in SDMR. The desired value can be set in SDMR by writing any value in this address.

Interface Circuit Diagram: Figure 2.7 shows an interface circuit for the case in which area 3 of the SH7708R is connected to SDRAM (HM5264165-B60) via a 32-bit bus.



Note: Upper addresses of the SH7708R, which are not multiplexed with other pin functions, are used for SDRAM bank selection. In thisinterface example, A22 and A23 of the SH7708R are used. The address multiplex bits (AMX) of MCR must be specified as AMX[1:0]=00.

Figure 2.7 Interface between SDRAM (HM5264165-B60) and SH7708R

2.3.4 Power-On Sequence (SH7708R)

To use the synchronous DRAM, specify modes after power-on. To initialize the synchronous DRAM correctly, first specify the bus state controller registers and then specify the synchronous DRAM mode register. When specifying the synchronous DRAM mode register, the address signal value is latched depending on the combination of $\overline{RAS}$, $\overline{CAS}$, and RD/$\overline{WR}$ signals. In this case, the bus state controller functions as follows. To write a designated value X to the DRAM mode register, write data to address H'FFFFD000 + X for area 2 of synchronous DRAM and write data to H'FFFFE000 + X for area 3 of synchronous DRAM. At this time, data written at addresses H'FFFFD000 + X and H'FFFFE000 + X is ignored and the DRAM mode register is written in byte units.

To specify burst read/single write, CAS latency as 1 to 3, sequential as lap type, and burst length as 1, write arbitrary data in byte units to the addresses listed below.

	Area 2	**Area 3**
CAS latency 1	FFFD840	FFFE840
CAS latency 2	FFFD880	FFFE880
CAS latency 3	FFFD8C0	FFFE8C0

By writing data to address H'FFFD000 + X or address H'FFFE000 + X, the precharge all banks command (PALL) is first issued at cycle TRp1, and a mode register write command is issued at the following cycle TMw1.

Before specifying the mode register, 100 µs of idle time (differs depending on the memory manufacturer) required for synchronous DRAM must be ensured after power-on. If the pulse width of the reset signal is longer than this idle time, the mode register can be specified immediately after power-on. In addition, dummy auto-refresh cycles must be executed for the number of times specified by the manufacturer (normally 8 times) or more. Dummy auto-refresh cycles are normally specified to be executed automatically during initializations after auto-refresh setting. However, to ensure execution of the auto-refresh cycles, the time intervals between refresh requests must be shortened while the dummy cycles are executed. Note that the auto-refresh cycles must be executed in order to initialize the synchronous DRAM internal address counter because the synchronous DRAM internal address counter cannot be initialized by a normal read or write access.

SH-3, SH3-DSP SDRAM Interface Applicarion Note

Publication Date: 1st Edition, February 2002
Published by: Semiconductor & Integrated Circuits
Hitachi, Ltd.
Edited by: Technical Documentation Group
Hitachi Kodaira Semiconductor Co., Ltd.